

PATENT ABSTRACTS OF JAPAN

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H01L 21/60
H01L 25/07
H01L 25/18

(21)Application number : 02-237713

(71)Applicant : MITSUBISHI ELECTRIC CORP

(22)Date of filing : 06.09.1990

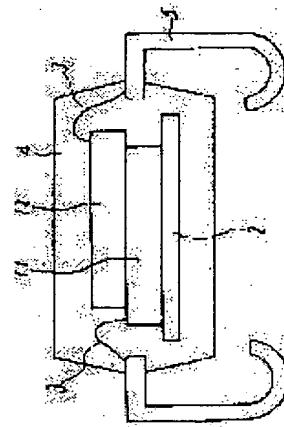
(72)Inventor : SAWANO HIROSHI

(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To reduce the size of a package by forming a chip wherein the circuit function of a semiconductor device is divided into two chips, and sealing said chips which are stacked in the same package.

CONSTITUTION: The title semiconductor device is formed by dividing a chip constituting a circuit into two chips, and sealing the divided chips which are stacked. Thereby a chip size is restrained and the defective rate can be decreased. Since the package size is reduced, the mounting area can be made small.



LEGAL STATUS

[Date of request for examination]

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[Date of extinction of right]

(Full translation)

Japanese Patent Application Laid-Open No. Hei 4(1992)-116859.

Laid-Open Date: April 17, 1992

Title of the Invention: Semiconductor device

Application No. Hei 2(1990)-237713

Application Date: September 6, 1990

Inventor: Hiroshi Sawano

Applicant: Mitsubishi Electric Corp.

Specification

1. Title of the Invention:

Semiconductor device

2. What is claimed is:

A semiconductor device characterized in that chips whose circuit functions are separated into two in the semiconductor device, are fabricated and encapsulated in the same package in their superimposed form to thereby reduce the size of the package to 1/2.

3. Detailed Description of the Invention:

[Industrial Field of Application]

The present invention relates to a semiconductor device.

[Prior Art]

Fig. 1 is a cross-sectional view of a conventional semiconductor device. Reference numeral (1) indicates a

chip, reference numeral (2) indicates a die pad, reference numerals (3) indicate wires, reference numeral (4) indicates an encapsulating resin, and reference numerals (5) are indications of external leads, respectively.

A configuration thereof will next be explained. In the semiconductor device, one chip has heretofore been encapsulated in one package and its function has been fulfilled. And the function has increasingly been brought into high integration and changed to a complex one or a large chip. Therefore, in a memory semiconductor device in particular, only the capacity thereof has heretofore been increased without changing the size of its package.

[Problems to be Solved by the Invention]

Since the conventional semiconductor device has made increases in its function and capacity without changing the size of its package, the semiconductor device became multifunctional and high in capacity, so that it became so easy to use. However, in order to make attainment with more multifunction and larger capacity, its limit has come into sight with only a reduction in chip's circuit. There has appeared a situation in which the package per se has no other choice to absolutely increase. When a dynamic memory is taken into consideration, for example, it can be encapsulated in the same package size up to a capacity of 1M but its encapsulation becomes impossible in part in the case of

4M. Increasing the chip size incurs even an increase in defective fraction, and the advantage of the semiconductor that its cost is reduced while the conventional multifunction and increase in capacity are being performed, has become close to the limits.

The present invention has been made to solve the foregoing problems. It is so desirable to take a reasonable chip size and a package size identical to the conventional one for the purpose of attaining multifunction and an increase in capacity at low cost.

[Means for Solving Problems]

In a semiconductor device according to the present invention, chips each constituting a circuit are separated into two to avoid an increase in chip size, and the divided chips are encapsulated with being superimposed on each other, whereby a package size is reduced.

[Effects]

The division of a chip size into two contributes to a reduction in defective fraction that increases in inverse proportional to the chip size due to a problem such as dust or the like. Owing to the superimposition of the chips, a reduction in package size is also achieved and hence an improvement in packaging density is obtained.

[Embodiments]

In Fig. 2, reference numerals (11) and (12) indicate chips divided into two, reference numeral (2)

indicates a die pad, reference numerals (3) indicate wires, reference numeral (4) indicates an encapsulating resin, and reference numerals (5) indicate external leads.

With the division of the chips into the two, an increase in chip size is avoided and a reduction in defective fraction is achieved. Further, a reduction in package size can be made owing to superimposition of these chips. Consequently, a packaging area can be less reduced, and particularly a system using a number of semiconductor devices such as a computer, etc. can be made so compact.

Incidentally, although a description has been made of the plastic package wherein the chip is placed on the chip in the figure, the chips may be mounted to both surfaces of the die pad or a ceramic package may be used.

[Advantages of the Invention]

Since chips are divided into two, a chip size per one is suppressed and a defective fraction can be reduced. With the superimposition of the chips, a package size can be reduced, thereby enabling a decrease in mounting area

4. Brief Description of the Drawings:

Fig. 1 is a cross-sectional view of a conventional one, wherein reference numeral (1) indicates a chip, reference numeral (2) indicates a die pad, reference numerals (3) indicate wires, reference numeral (4) indicates an encapsulating resin, and reference numerals (5) indicate external leads respectively. Fig. 2 is a

cross-sectional view of a semiconductor device according to the present invention, wherein reference numerals (11) and (12) indicate chips, reference numeral (2) indicates a die pad, reference numerals (3) indicate wires, reference numeral (4) indicates an encapsulating resin, and reference numerals (5) indicate external leads respectively.

Incidentally, the same reference numerals in the figures indicate the same or corresponding portions respectively.

Agent: Masuo Ooiwa

AMENDMENT (VOLUNTARY)

December 18, 1990

To: Director-General

Patent Office

1. Identification of the Case:

Patent Application No. 237713/1990

2. Title of the Invention:

Semiconductor device

3. Person Attending To the Amendment:

Relationship with the Case: Applicant for Patent

Address: 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo

Name: (601) Mitsubishi Electric Corp.

Representative: Moriya Shiki

4. Agent:

Address: 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo

c/o Mitsubishi Electric Corp.

Name: Ooiwa Masuo, Patent Attorney

(Reg'n No. 7375)

(Patent Dept/contact: 03(213)3421)

5. Places Subjected to the Amendment:

In the specification, "Detailed Description of the Invention".

6. Details of the Amendment:

(1) In the specification, page 1, line 15, amend
"(5) are indications of external leads" to "(5) indicate
external leads".

(2) In the specification, page 1, line 20, amend

"... a large chip. Therefore, in a memory semiconductor device in particular," to "... a large chip. In a memory semiconductor device in particular".

(3) In the specification, page 2, line 5, amend "Since the conventional semiconductor device has made increases in its function and capacity ..." to "Since the conventional semiconductor device has been increased in its function and capacity ...".

(4) In the specification, page 2, line 7, amend "However, in order to make attainment with more multifunction and larger capacity," to "However, in order to attain more multifunction and larger capacity".

- Concluded -

⑯日本国特許庁 (JP) ⑮特許出願公開
⑰公開特許公報 (A) 平4-116859

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25/07
25/18

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301 B 6918-4M

⑯公開 平成4年(1992)4月17日

7638-4M H 01 L 25/08

審査請求 未請求 請求項の数 1 (全3頁) B

④発明の名称 半導体装置

⑦特 願 平2-237713

⑦出 願 平2(1990)9月6日

⑦発明者 沢 野 寛 兵庫県伊丹市瑞原4丁目1番地 三菱電機株式会社北伊丹
製作所内

⑦出願人 三菱電機株式会社 東京都千代田区丸の内2丁目2番3号

⑦代理人 弁理士 大岩 増雄 外2名

明細書

1. 発明の名称

半導体装置

2. 特許請求の範囲

半導体装置において回路の機能を2分割したチップを作り、そのチップを同一パッケージ内に重ね合せて封止する事によりパッケージの大きさを1/2に削減する事を特徴とした半導体装置。

3. 発明の詳細な説明

〔産業上の利用分野〕

この発明は半導体装置に関するものである。

〔従来技術〕

図1は従来の半導体装置の断面図であり、(1)はチップ、(2)はダイパッド、(3)はワイヤ、(4)は封止樹脂、(5)は外部リード示す。

次にこの構成について説明する。従来は半導体装置は一つのパッケージ内に一つチップを封止してその機能を発揮して来た。そしてその機能はどんどんと高集積化され複雑なものに又大きなチップに変わってきた。この為、特に記憶用半導体装

置では従来、パッケージの大きさは変化させないで容量のみの増加を図ってきた。

〔発明が解決しようとする課題〕

従来の半導体装置はパッケージの大きさを変えないで機能容量を増加を図って来ての多機能、高容量となり大変使いやすかった。が一層の多機能、大容量で達成するにはチップの回路の縮小だけでは限界が見えており、どうしてもパッケージそのものも大きくせざるを得ない状況となつて来た。例えばダイナミックメモリを考えた場合、1Mの容量迄は同一のパッケージサイズに封止可能であったが4Mでは一部不可能となつた。又チップサイズの増大は不良率の増加もまねき、これ迄の多機能、大容量化を行ないながらコストダウンを行う半導体の長所が限界に近くなつて来た。

この発明は上記の様な問題を解決する事になされたものである。多機能、大容量化を安価に達成するには程良いチップサイズ従来と同じパッケージサイズが大変好ましい。

〔問題を解決するための手段〕

この発明における半導体装置は回路を構成するチップを2分割しチップサイズの大形化を避け、又分割したチップを重ね合せて封止する事によりパッケージサイズの減少を図っている。

【作用】

チップサイズの2分割はゴミ等の問題によりチップサイズに逆比例して増大する不良率の低減に寄与し、かつ重ね合せた事によりパッケージサイズの減少にもなり、実装密度の向上が得られる。

【実施例】

図2において(1)と(2)は2分割されたチップであり、(3)はダイパッド、(4)はワイヤ、(5)は封止樹脂、(6)は外部リードを示す。

チップを2分割する事によりチップサイズの大形化を避け不良率の低減を図り、かつそれらのチップを重ね合せる事によりパッケージサイズの減少が行え、これにより実装面積が少なくなり、特にコンピュータ等の多數の半導体装置を使用するシステムでは大変コンパクトにする事が可能である。

なお図ではチップの上にチップを乗せたプラスチックパッケージで説明したが、ダイパッドの両面に取り付けてもしく又セラミックパッケージでも可能である。

【発明の効果】

チップを2分割したので1ヶ当りのチップサイズが抑えられ不良率が減少でき、かつ重ね合せた事によりパッケージサイズが減少できる事により実装面積が小さくできる。

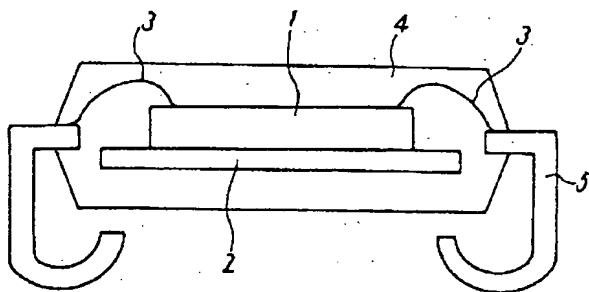
4. 図面の簡単な説明

第1図は従来のものの断面図であり、(1)はチップ、(2)はダイパッド、(3)はワイヤ、(4)は封止樹脂、(5)は外部リードを示す。第2図は本発明による半導体装置の断面図であり、(1)、(2)はチップ、(3)はダイパッド、(4)はワイヤ、(5)は封止樹脂、(6)は外部リードを示す。

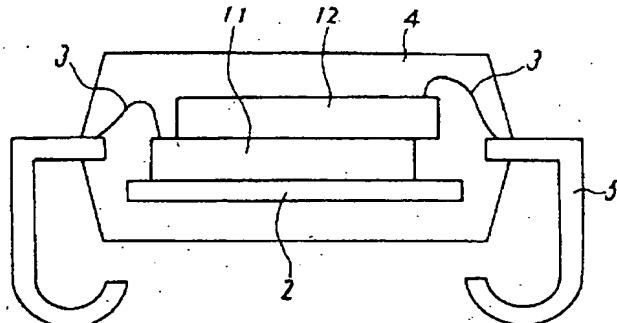
なお、図中、同一符号は同一、または相当部分を示す。

代理人 大岩増雄

第1図



第2図



手 線 補 正 書(自発)

平成2年12月18日

特許庁長官殿

通

1. 事件の表示

平特願昭2-237713号

2. 発明の名称

半導体装置

3. 補正をする者

事件との関係 特許出願人

住 所 東京都千代田区丸の内二丁目2番3号

名 称 (601)三菱電機株式会社

代表者 志岐守哉

4. 代 理 人

東京都千代田区丸の内二丁目2番3号

三菱電機株式会社内

氏 名 (7375)弁理士 大岩増雄

(連絡先03(213)3421特許部)



5. 精正の対象

明細書の発明の詳細な説明の欄

6. 精正の内容

(1) 明細書第1頁第15行の

「(5)は外部リード示す。」を

「(5)は外部リードを示す。」と訂正する。

(2) 明細書第1頁第20行の

「来た。この為、特に」を

「来た。特に」と訂正する。

(3) 明細書第2頁第5行の

「増加を図って来るので」を

「増加を図って来たので」と訂正する。

(4) 明細書第2頁第7行の

「大容量で達成するには」を

「大容量を達成するには」と訂正する。

以上